Amendments to the claims

Please amend claims 1, 17, 23 and 24 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) A phase-locked loop (PLL) comprising:

a voltage controlled oscillator including a varactor having a first set of capacitor cells configured to adjust a capacitance based on a first control voltage, and a second set of capacitor cells configured to adjust a capacitance based on a second control voltage; and

a charge-pump loop filter configured to receive a first and a second update signal each having at least one state based on a phase difference between a first clock and a second clock, and comprising:

a first component configured to adjust, during an update period, a voltage across an impedance from a reference level based on the states of the first and second update signals and to return the voltage across the impedance to the reference level prior to an end of the update period, wherein the voltage across the impedance comprises the first control voltage; and

a second component configured to adjust a voltage across a capacitor based on the states of the first and second input signals, wherein the voltage across the capacitor comprises the second control voltage.

2. (original) The PLL of claim 1, wherein the impedance comprises a capacitor.

3. (original) The PLL of claim 1, wherein the first clock comprises an input reference clock and the second clock comprises a feedback clock.

4. (original) The PLL of claim 1, wherein the first control voltage is substantially proportional to the phase difference.

5. (original) The PLL of claim 1, wherein the second control voltage is substantially proportional to an integral of the phase difference.

6. (original) The PLL of claim 1, wherein the first control voltage adjusts a phase of the second clock.

7. (original) The PLL of claim 1, wherein the second control voltage adjusts a frequency of the second clock.

8. (original) The PLL of claim 1, wherein the update period comprises a clock period of the first clock.

9. (original) The PLL of claim 1, wherein the voltage across the impedance has a level adjusted from the reference level for a duration based on the first and second clocks.

10. (original) The PLL of claim 1, wherein the first component is configured to provide the first control voltage at a level substantially equal to ground in response to a first test signal and substantially equal to a power supply voltage in response to a second test signal, and wherein the second component is configured to provide the second control voltage at a level substantially equal to ground in response to a first test signal and substantially equal to a power supply voltage in response to a second test signal.

11. (original) The PLL of claim 1, wherein the first component comprises:

a first current source coupled to a power supply voltage;

a first switch coupled between the first current source and an output node, and configured to open and close based on the first update signal;

a second current source coupled to ground;

a second switch coupled between the second current source and the output node, and configured to open and close based on the second update signal;

a capacitor coupled between the supply node and ground, wherein a voltage across the capacitor comprises the first control voltage;

a NOR-gate receiving the first and second clocks at a pair of inputs and providing a reset signal at an output; and

a third switch coupled between the output node and a reference voltage and configured to open and close based on the reset signal.

12. (original) The PLL of claim 11, wherein the first current source provides a current from the voltage source to the output node when the first switch is closed, and the second current source provides a current from the output node to ground when the second switch is closed.

13. (original) The PLL of claim 1, wherein the second component comprises:

a first current source coupled to a power supply voltage;

a first switch coupled between the first current source and an output node, and configured to open and close based on the first update signal;

a second current source coupled to ground;

a second switch coupled between the second current source and the output node, and configured to open and close based on the second update signal; and

a capacitor coupled between the output node and ground, wherein a voltage across the capacitor comprises the second control voltage.

14. (original) The PLL of claim 13, wherein the first current source provides a current from the voltage source to the output node when the first switch is closed, and the second current source provides a current from the output node to ground when the second switch is closed.

15. (original) The PLL of claim 1, where in the charge pump loop filter comprises:

a plurality of first components, each configured to adjust, during the update period, a voltage across a corresponding impedance from a reference level based on the state of the first and second update signals and to return the voltage across the impedance to the reference level prior to the end of the update period, wherein the voltage across the impedance comprises a corresponding first control voltage for controlling a corresponding set of capacitor cells of the voltage

controlled oscillator, and wherein each of the first components of the plurality of first components is configured to be selectively enabled or disabled to adjust a phase lead compensation of the PLL.

16. (original) The PLL of claim 1, wherein the charge pump loop filter comprises:

a plurality of second components, each configured to adjust a voltage across a capacitor based on the states of the first and second input signals, wherein the voltage across the capacitor comprises a corresponding second control voltage for controlling a corresponding set of capacitor cells of the voltage controlled oscillator, and wherein each of the second components is configured to be selectively enabled or disabled.

17. (currently amended) A charge-pump loop filter for a phase-locked loop including voltage controlled oscillator including a varactor having a first set of capacitor cells configured to adjust a capacitance based on a first control voltage, and a second set of capacitor cells configured to adjust a capacitance based on a second control voltage, the charge-pump loop filter configured to receive a first and a second update signal each having at least one state based on a phase difference between a first clock and a second clock, the charge-pump loop filter comprising:

a first component configured to adjust, during an update period, a voltage across a first capacitor from a reference level based on the states of the first and second update signals and to return the voltage across the first capacitor to the reference level prior to an end of the update period, wherein the voltage across the first capacitor comprises the first control voltage; and

a second component configured to adjust a voltage across a second capacitor based on the states of the first and second input signals, wherein the voltage across the second capacitor comprises the second control voltage.

18. (original) The charge-pump loop filter of claim 17, wherein the first control voltage is substantially proportional to the phase difference.

19. (original) The PLL of claim 17, wherein the second control voltage is substantially proportional to an integral of the phase difference.

20. (original) The PLL of claim 17, wherein the first control voltage adjusts a phase of the second clock.

21. (original) The charge-pump loop filter of claim 17, wherein the second control voltage adjusts a frequency of the second clock.

22. (original) The charge-pump loop filter of claim 17, wherein the update period comprises a clock period of the first clock.

23. (currently amended) A method of operating a charge-pump phase-locked loop having a voltage controlled oscillator including a varactor having a first set of capacitor cells configured to adjust a capacitance based on a first control voltage, and a second set of capacitor cells configured to adjust a capacitance based on a second control voltage, the method comprising:

receiving a first and second update signal each having at least one state based on a phase difference between a first clock and a second clock;

providing the first control voltage having a level substantially proportional to the phase difference, including adjusting, during an update period, a voltage across an impedance from a reference level based on the states of the first and second update signals and to return the voltage across the impedance to the reference level prior to an end of the update period, wherein the voltage across the impedance comprises the first control voltage; and

providing the second control voltage having a level substantially proportional to an integral of the phase difference clock.

24. (currently amended) The method of claim 23, wherein said impedance comprises a capacitor ~~providing the first control voltage comprises:~~

~~adjusting, during an update period, a voltage across a capacitor from a reference level based on the states of the first and second update signals and to return the voltage across the capacitor to the reference level prior to an end of the update period, wherein the voltage across the capacitor comprises the first control voltage~~.

25. (original) The method of claim 23, wherein providing the second control voltage comprises:

adjusting a voltage across a capacitor based on the states of the first and second input signals, wherein the voltage across the capacitor comprises the second control voltage.